

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
12 May 2005 (12.05.2005)

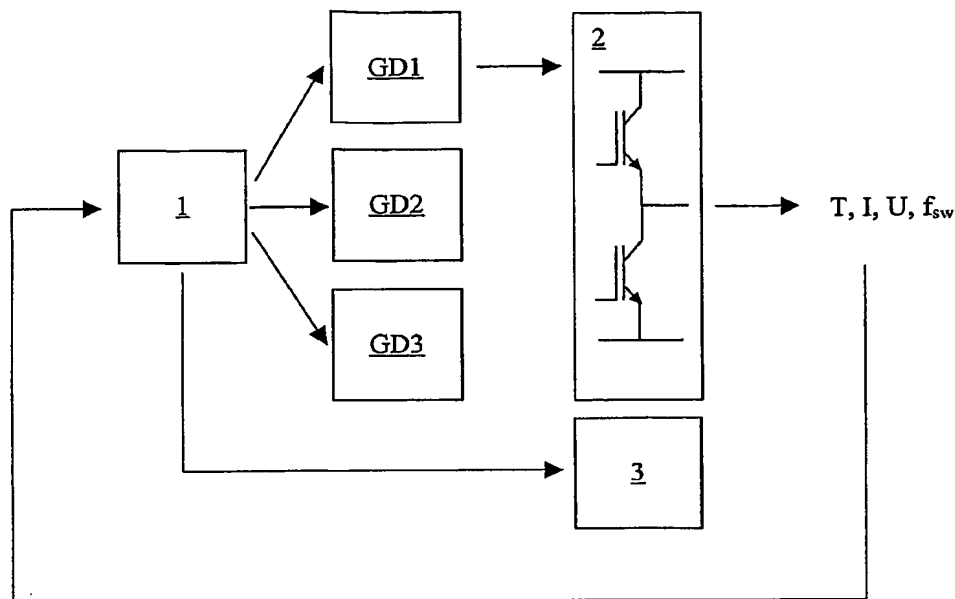
PCT

(10) International Publication Number  
**WO 2005/043618 A1**

- (51) International Patent Classification<sup>7</sup>: **H01L 23/34, H02M 5/00, G01K 3/00**
- (21) International Application Number: **PCT/FI2004/000642**
- (22) International Filing Date: 29 October 2004 (29.10.2004)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
20031580 30 October 2003 (30.10.2003) FI
- (71) Applicant (for all designated States except US): **ABB OY** [FI/FI]; Strömbergintie 1, FI-00380 Helsinki (FI).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **RONKAINEN, Teemu** [FI/FI]; Taavintörmä 6 B, FI-02180 Espoo (FI). **HYVÄRINEN, Veikko** [FI/FI]; Länsipellontie 3, FI-00390 Helsinki (FI). **TIITINEN, Pekka** [FI/FI]; Aitaintie 22 A, FI-01390 Vantaa (FI).
- (74) Agent: **KOLSTER OY AB**; Iso Roobertinkatu 23, P.O. Box 148, FI-00121 Helsinki (FI).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: METHOD AND ARRANGEMENT IN INVERTER



(57) Abstract: A method and arrangement in connection with an inverter that comprises several power semiconductor components and a control apparatus arranged to control them, the control apparatus being arranged to control the power semiconductor components in response to a control quantity to generate an output voltage. The method comprises the steps of determining the change of the temperature or a quantity affecting the temperature of one or more power semiconductor components, and controlling with the control apparatus the power semiconductor components in response to both the control quantity to generate an output voltage and the change rate of the temperature or quantity affecting the temperature of the power semiconductor components to reduce the temperature change and the change rate.

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**Declarations under Rule 4.17:**

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE,

BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

- of inventorship (Rule 4.17(iv)) for US only

**Published:**

- with international search report

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